Amendments to Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method of manufacturing an integrated circuit having trench isolation regions in a substrate including a first layer, the method comprising:

selectively etching the first layer to form apertures associated with locations of the trench isolation regions;

forming strained semiconductor material above the first layer; and

forming insulative material in the apertures to form the trench isolation regions.

2. (Original) The method of claim 1, wherein the strained semiconductor material is formed on sidewalls of the apertures.

3. (Withdrawn) The method of claim 1, wherein strained semiconductor material is formed after the insulative material is formed.

4. (Original) The method of claim 1, wherein the strained semiconductor material is formed before the insulative material is formed.

5. (Withdrawn) The method of claim 3, wherein the strained semiconductor material is formed by selective epitaxial growth.

6. (Original) The method of claim 1, further comprising:

siliciding the strained semiconductor material.

7. (Original) The method of claim 1, wherein the strained semiconductor material is silicon and the first layer is silicon-germanium.

8. (Original) The method of claim 1, wherein the first layer is above a BOX layer.

9 - 24. (Cancelled)

25. (New) A method of manufacturing an integrated circuit comprising:

forming trenches in a substrate comprising a germanium-containing layer;

providing a strained semiconductor material above the germanium-containing layer and on sidewalls of the trenches; and

providing insulative material in the apertures to form trench isolation regions.

26. (New) The method of claim 25, wherein the strained semiconductor material is formed on sidewalls of the trenches.

27. (New) The method of claim 25, further comprising siliciding the strained semiconductor material.

28. (New) The method of claim 25, wherein the germanium-containing layer comprises a silicon-germanium material.

29. (New) The method of claim 25, wherein the strained semiconductor material comprises strained silicon.

30. (New) The method of claim 25, wherein the insulative material comprises silicon dioxide.

31. (New) The method of claim 25, wherein the first layer is above a buried oxide layer.

32. (New) The method of claim 31, wherein the trenches extend through the germanium-containing layer to the buried oxide layer.

33. (New) A method of producing an integrated circuit comprising:

forming a trench having sidewalls in a substrate comprising a silicon-germanium layer;

forming a strained silicon material above the silicon-germanium layer and on the sidewalls of the trench; and

filling the trench with an insulative material to form a trench isolation region.

34. (New) The method of claim 33, wherein the strained silicon material is formed on sidewalls of the trenches.

35. (New) The method of claim 33, further comprising siliciding the strained silicon material.

36. (New) The method of claim 33, wherein the trench extends through the silicon-germanium layer to an underlying buried oxide layer.